Signal Processing for High Granularity Calorimeter: Amplification, Filtering, Memorization and Digitalization

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***Abstract*—A very-front-end electronics dedicated to high granularity calorimeters has been designed and its performance measured. This electronics performs the amplification of the charge delivered by the detector thanks to a low-noise Charge Sensitive Amplifier. The dynamic range is improved using a bandpass filter based on a gated integrator. Studying its weighting function, we show that this filter is more efficient than standard CRRC shaper, thanks to the time of integration which can be expand near the bunch interval time, whereas the peaking time of the CRRC shaper is limited to pile-up consideration. Moreover, the gated integrator performs intrinsically the analog memorization of the signal before its delayed digital conversion. The analog-to-digital conversion is performed through a 12-bit cyclic ADC specifically developed for this application.**
The very-front-end channel has been fabricated using a 0.35 μm CMOS technology. Measurements show a global non-linearity better than 0.1 %. The Equivalent Noise Charge at the input of the channel is evaluated to 1.8 fC, compare to the maximum input charge of 10 pC. The power consumption of the complete channel is limited to 6.5 mW.

***Index Terms*—CMOS, very-front-end electronics, integrated circuit, charge sensitive amplifier, CSA, shaper, gated integrator, cyclic ADC, calorimeter.**

I. Introduction

In order to explore the new physics beyond the standard model, the next generation of particle detector has to achieve unprecedented particle identification and separation [1]. Highly granular calorimeter are required and numerous ambitious R&D are in progress, both on detector and electronics, to reach the required performance. The Very-Front-End (VFE) electronics associated to this kind of detector has to process a large number of channels (up to several millions) with a wide dynamic range (about 80 dB) and a precision better than 1%. The signal delivered by each channel of the detector has to be amplified, filtered, memorized and digitalized. Moreover, the compactness of the calorimeter and its large number of channels impose a drastic limitation of the power consumption of the VFE and its high level of integration.

This paper presents the design and the performance of a complete readout channel dedicated to high granularity calorimeters. This VFE channel represented in Fig.1 is composed of a low-noise Charge Sensitive Amplifier (CSA) followed by a shaping stage. The shaper is made of a Gated Integrator (GI) which includes an intrinsic analog memory thanks to the integration capacitor. The final analog-to-digital conversion is performed by a low-power 12-bit cyclic ADC. This paper is organized as follows. In Section 2 the Charge Sensitive Amplifier is described, and Section 3 is devoted to the shaping stage where the filtering performance of the Gated Integrator is compare to the performance of the standard CRRC shaper. After the description of the cyclic ADC in Section 4, the results of measurements done on the VFE channel are presented in Section 5 before to conclude.

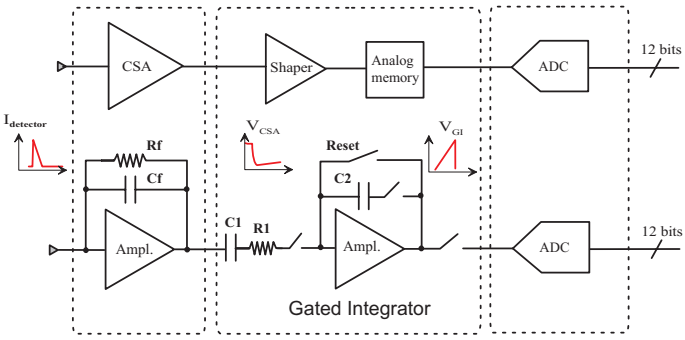

Fig. 1. The VFE channel designed: the CSA is followed by a Gated Integrator which performs the shaping and the memorization of the analog signal; the last stage is a 12-bit cyclic ADC.

II. The Charge Sensitive Amplifier

The structure of the CSA is presented in Fig. 2 with a schematic view of the amplifier block itself. The CSA is designed to process a signal up to a charge of 10 pC. The output voltage of the preamplifier is proportional to the input charge divided by the feedback capacitance as reported in Eq. 1

$$V_{out} = \frac{-Q}{C_f + \frac{C_d}{G_{OL}}} \tag{1}$$

with Q the charge delivered by the detector, C_d and C_f respectively the detector and the feedback capacitors, and G_{OL} the open loop gain of the amplifier. With a high value of gain G_{OL}, the output voltage of the SCA is proportional to the collected charge as follow:

$$V_{out} \approx -Q/C_f \tag{2}$$

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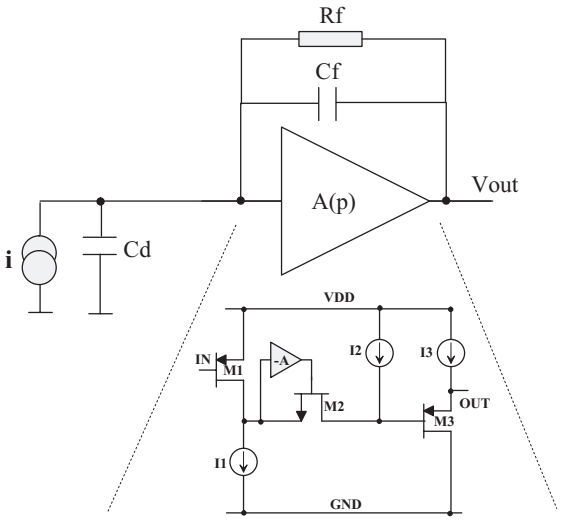

Fig. 2. Architecture of the CSA with the schematic view of the boosted folded cascode amplifier

To reach the high gain value required, the amplifier is based on a boosted folded cascode architecture as represented in Fig. 2, followed by a source follower. At low frequency, its open loop gain value can be approximated as:

$$G_{OL} \approx -gm_1 \times r_{I_2} \tag{3}$$

where gm_1 is the transconductance of the input PMOS transistor M_1 and r_{I_2} the equivalent resistance of the current generator I_2.

Main characteristics of the CSA with a power consumption of 3.54 mW are reported in Table I. The Equivalent Noise Charge (ENC) at the input of the CSA is limited to a RMS value of 0.5 fC when this CSA is associated to a noise-free CRRC shaper with a peaking time of 200 ns. This ENC value gives a dynamic range of 80 dB if the Minimum-Ionizing Particle (MIP) is fixed to twice the level of noise.

TABLE I
MAIN CHARACTERISTICS OF THE CSA (SIMULATED RESULTS).

Power supply	3.3 V
Consumption	3.54 mW
$C_{Detector}$	30 pF
$C_{Feedback}$	10 pF
Transconductance gm_1	7 mΩ^{-1}
Open Loop Gain G_{OL}	83 dB
Gain-Band Width	105 MHz
Output swing	1.0 V
ENC (with a 200 ns CCRC shaper)	0.5 fC
Dynamic range	80 dB

III. Noise Considerations and Shaping

The dynamic range of the readout channel is one of the key issues for calorimetry. It is defined as the ratio between the largest recordable signal and the smallest detectable signal above the level of noise. In order to improve this dynamic range, the level of noise has to be attenuate thanks to an optimized bandpass filtering. The relative performances of a time-variant filter and a time-invariant filter are evaluated by simulation.

A. Sources of Noise

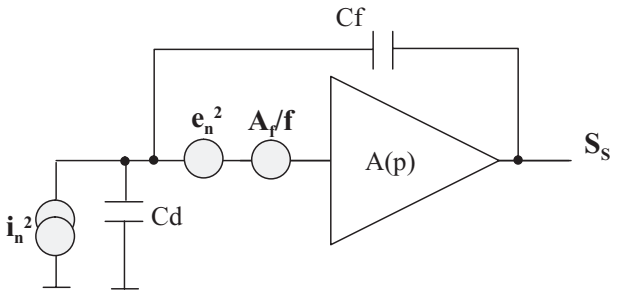

Fig. 3. Equivalent sources of noise at the CSA input: two serial (voltage) sources and one parallel (current) source.

The three equivalent sources of noise at the input of the CSA are represented in Fig. 3 and the spectral density of this noise at the output of the CSA is evaluated by relation

$$S_S(\omega) = \frac{i_n^2}{\omega^2 \cdot C_f^2} + \left(1 + \frac{C_d}{C_f}\right)^2 \cdot \left(e_n^2 + \frac{A_f}{f}\right) \tag{4}$$

where i_n corresponds to the shot noise generated by the input transistor's gate leakage current, e_n is the thermal noise introduced by the preamplifier and A_f is the process dependant flicker noise parameter [2]. The term $\left(e_n^2 + \frac{A_f}{f}\right)$ corresponds to the equivalent spectral density of the serial (voltage) noise observed at the input of the CSA, and i_n^2 the parallel (current) counterpart. The efficiency of a filter has to be evaluated both for serial and parallel noises.

B. Noise Index Analysis

As the gated integrator is a time-variant filter, the relative noise performance of the CRRC shaper and of the gated integrator can not be compared using their frequency transfer functions, but using their corresponding weighting functions $R(t)$ in a time domain analysis. The weighting function is the measurement of influence of a noise step generated before the measuring time on the amplitude at the measuring time [3], [4]. It can be estimated with a simulation through the Virtuoso tools from Cadence. The two channels of filtering simulated for comparison are represented in Fig. 4. To limit the contribution of the low-frequency noise, a basic exponential pre-filter with components (C_3, R_3) is used at the input of the gated integrator.

The parameters of the CRRC shaper are:

- Derivator: $R_1 = 40\,k\Omega, C_1 = n \times 5\,pF$.
- Integrator: $R_2 = 140\,k\Omega, C_2 = n \times 0.83\,pF$.

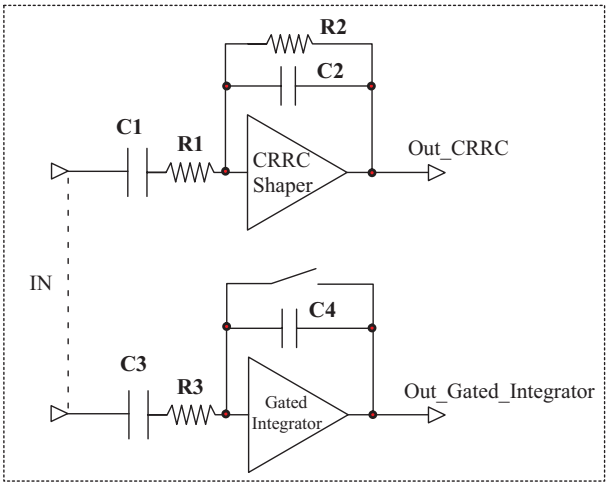

Fig. 4. Simulated schematic view, with CRRC shaper on the top and Gated Integrator at the bottom.

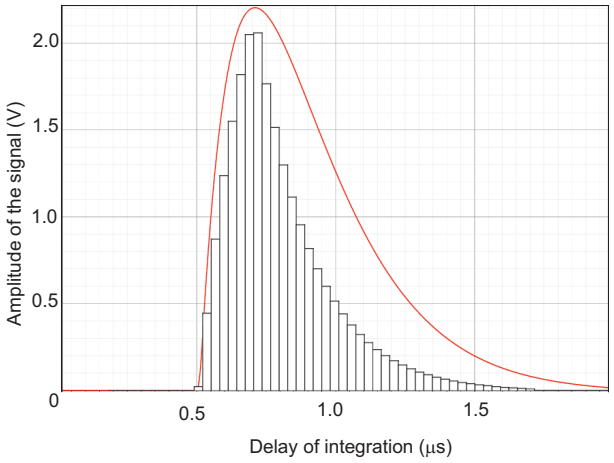

Fig. 5. Weighting functions of the CRRC (full line) and of the gated integrator (histogram) with a peaking time and duration of integration of 200 ns.

where the peaking time τ_p depends to the value of the parameter n with $\tau_p\,(ns) = n \times 200$.

The weighting function of the CRRC shaper is directly provided by its transfer function expressed as:

$$R_{CRRC}(t) = \frac{t}{\tau_p} \cdot e^{(1-\frac{t}{\tau_p})} \tag{5}$$

Concerning the gated integrator, the time of integration can be tuned whereas the constant time of the exponential pre-filter is fixed to 200 ns with the components R_3=40 kΩ and C_3=5 pF. To obtain a DC voltage gain similar to the CRRC shaper one, the capacitor value of the integrator is fixed to C_4=1.45 pF.
The weighting function $R_{G.I.}(t)$ of the gated integrator is obtained by simulation using the technique given by F.S. Goulding [3]. The integration interval T_I is slid over the whole signal waveform with 50 successive delayed transient simulations. The result at the end of each integration is stored and the plot of these values versus the delay time gives the curve of the weighting function. The weighting functions obtained are reported on Fig. 5.

The noise performances of each pulse-shaper is evaluated through the step-noise and delta-noise indices [3]. The step-noise index $< N_S^2 >$ corresponds to the parallel noise, whereas the delta-noise index $< N_\Delta^2 >$ evaluates the parallel noise performance of the shaper, with:

$$< N_S^2 >= \frac{1}{A^2} \int_0^\infty [R(t)]^2\, dt \tag{6}$$

$$< N_\Delta^2 >= \frac{1}{A^2} \int_0^\infty [R'(t)]^2\, dt \tag{7}$$

where A is the gain of the shaping function.
The indices for parallel and serial noises have been simulated for several values of peaking time τ_p (CRRC shaper) and several times of integration T_I (Gated Integrator). Results are reported on Fig. 6,7. They are in accordance with those obtained by [5] with a single gated-integrator coupled to an exponential pre-filter. We can observed that the serial noise index becomes lower for CRRC shaper when its peaking time is higher than 300 ns, whereas the parallel noise is lower with the gated integrator from a time of integration of 100 ns. For pile-up consideration, the peaking time of CRRC shaper must be limited to a fraction of the time interval between bunch crosses, whereas the fast resetting of the G.I. allows much larger time of integration. With a peaking time limited to 200 ns for the CRRC shaper and a time of integration up to 300 ns for the G.I., both serial and parallel noise indexes are reduced by about 30% with the G.I. filtering.

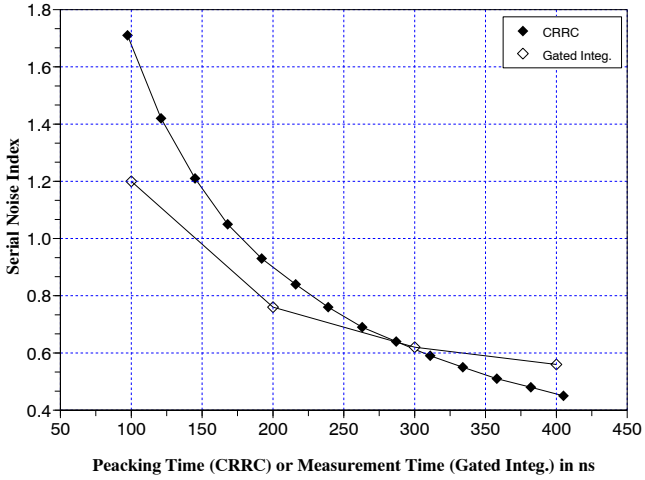

Fig. 6. Variation of the delta (serial) noise index for the CRRC shaper and the gated integrator versus the peaking time or the time of integration.

IV. The Analog-to-Digital Converter

The ADC implemented is the VFE channel is based on the converter described in [6]. The cyclic architecture is well adapted to compact-low-power converter. Its summarized performance is reported in Table II. The power consumption is limited to 1.5 mW with a time of conversion of 6.8 μs and a precision better than 10 bits.

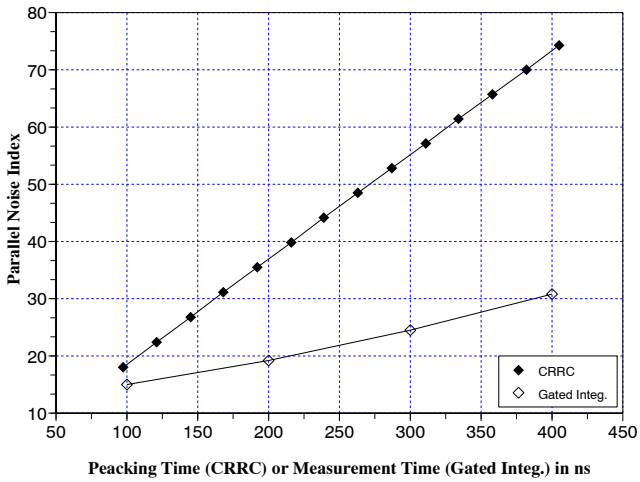

Fig. 7. Variation of the step (parallel) noise index for the CRRC shaper and the gated integrator versus the peaking time or the time of integration..

TABLE II
SUMMARIZED PERFORMANCE OF THE CYCLIC ADC (MEASUREMENTS RESULTS).

Architecture	1.5-bit/stage
Area	0.12 mm^2
Supply Voltage	3.0 V
Resolution	12 bits
Dynamique range	2.0 V differential
Time of conversion	6.8 μs
Consumption	1.5 mW
INL	3 LSB
RMS Noise	0.3 LSB

V. MEASUREMENTS RESULTS

A prototype chip has been fabricated using the Austriamicrosystems 0.35 μm 2-poly 4-metal CMOS process. Measurements of the VFE channel with the G.I. shaper have been carried out in order to evaluate linearity and noise. The time of integration T_I is fixed to 200 ns. It should be noted that the process of the bits delivered by the ADC has been implemented in an external programmable digital component. As plotted in Fig. 8, the error of linearity is within $\pm 4\, fC$ up to an input charge of 9.5 pC.

ADC code occurrence histogram with no input charge is given in Fig. 9. The standard deviation of this distribution is equal to 0.76 LSB it means 370 μV. The Equivalent Noise Charge (ENC) at the input of the channel is then lower to 2 fC.

The power of noise at the output of the channel, it means at the output of the ADC, is given in Fig. 10 for various values of time of integration. The curve obtained presents a decrease similar to the serial noise index curve given by simulation. It means that, in our design, the noise is dominated by the serial part up to time of integration higher than 400 ns.

Main performance of the VFE channel is reported in Table III.

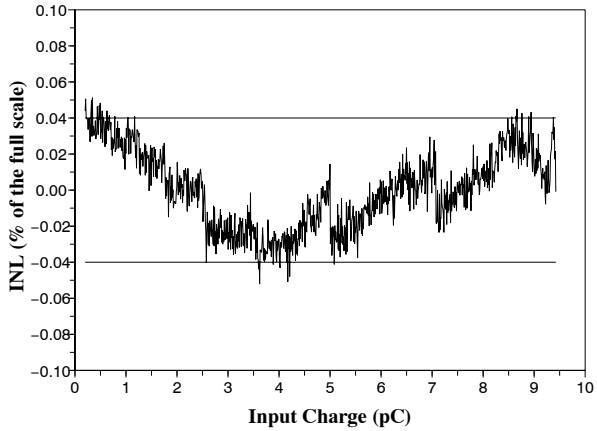

Fig. 8. Integral Non-Linearity of channel with Gated Integrator.

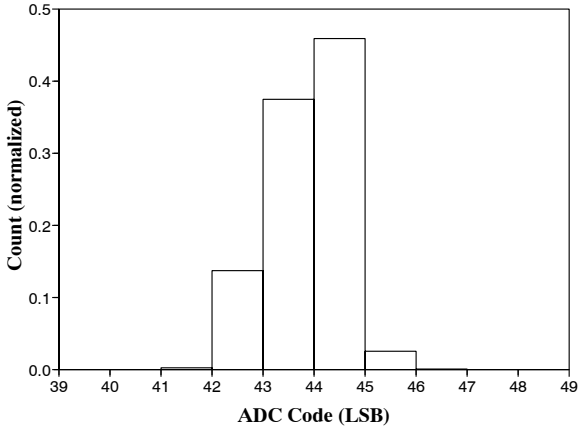

Fig. 9. Distribution of the code delivered by the ADC at the end of the VFE channel.

TABLE III
MAIN PERFORMANCE OF THE VFE CHANNEL WITH G.I..

Power supply	3.3 V
Consumption	6.5 mW
T_I Time of integration T_I	200 ns
Maximum input charge	10 pC
INL	$\pm 0.04\%$, $\pm$ 4 fC
ENC ($C_{Detector}$=30 pF)	1.8 fC

VI. CONCLUSION

A VFE electronics channel has been presented. It is dedicated to high-granularity calorimeter where low-power, high-integration electronics is mandatory. First, this channel performs the low-noise charge-sensitive amplification of the charge delivered by the detector. To improve the signal-to-noise ratio, the signal is then filtered thanks to a Gated Integrator. The study of the weighting function and the measurements of the gated integration show that this filtering is a performant alternative to CRRC shaping. Moreover, as the Gated Integrator includes intrinsically an analog memory, it can be used to memorise the voltage signal before its digitalization.

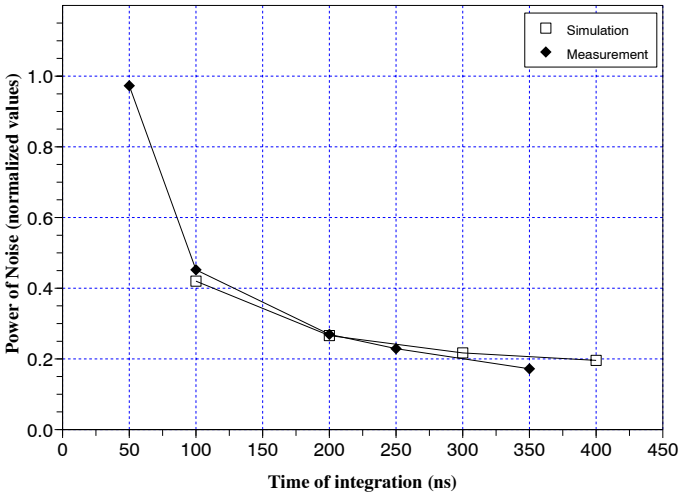

Fig. 10. Variation of the noise versus the time of integration of the G.I. obtained by simulation and by measurement.

The analog-to-digital conversion is lastly performed by a low-power 12-bit cyclic ADC fully customized for this application. Measurements of the prototype chip give a global linearity of the readout channel better than 0.1%. The Equivalent Noise Charge at the input of the channel is limited to a value of 1.8 fC which gives a signal-to-noise ratio of 75 dB considering a maximum input charge of 10 pC . The power consumption is limited to 6.5 mW and can be reduced with the implementation of a power pulsing system in accordance with the duty cycle of the beam sequence.

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